



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,950	12/10/2003	Woong-Kwon Kim	10125/4132	6763

7590 08/12/2008  
Brinks Hofer Gilson & Lione  
Post Office Box 10395  
Chicago, IL 60610

EXAMINER
----------

NGUYEN, HOAN C

ART UNIT	PAPER NUMBER
----------	--------------

2871

MAIL DATE	DELIVERY MODE
-----------	---------------

08/12/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/731,950	<b>Applicant(s)</b> KIM ET AL.	
	<b>Examiner</b> HOAN C. NGUYEN	<b>Art Unit</b> 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 15 May 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-54 is/are pending in the application.
- 4a) Of the above claim(s) 47 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-46 and 48-54 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Response to Amendment*

Applicant's arguments with respect to claims 1, 18, 35 and 46 based on the Response filed on 05/15/2008 have been considered but are moot in view of the new ground(s) of rejection. Therefore, this is Final action.

AMENDMENTS TO THE DRAWINGS has not been received by this office. Please resubmit the attached sheets of drawings include changes to FIG. 5 in the next response.

Claim 47 is withdrawn. Claims 55-59 are cancelled.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 4-12, 18, 21-31, 35, 37-41 and 48-54 are rejected under 35 U.S.C. 102(b) as being anticipated by **Yamamoto et al. (US6445432B2)**.

**Yamamoto et al.** teach (Figs. 2-4) a liquid crystal display device comprising:

Claims 1, 18, 35 and 46:

Art Unit: 2871

- a plurality of gate lines 3a formed on a first substrate along a transverse direction, each gate line including a gate electrode 3;
- a first insulating layer (gate insulating layer 4) formed on the first substrate to cover the gate lines and the gate electrodes;
- a plurality of data lines 6a formed on the first insulating layer along a longitudinal direction, the data lines defining a plurality of pixel regions with the gate lines and each including a source electrode 6;
- a thin film transistor formed at a crossing region of each of the gate and data lines, each thin film transistor including one of the gate electrodes, a semiconductor layer 5, one of the source electrodes, and a drain electrode;
- a color filter R over the first insulating layer in each pixel region, each color filter having one of red, green and blue colors R/G/B, the color filters having a plurality of drain contact holes exposing the drain electrodes 7;
- a pixel electrode 15 over the color filter in each pixel region, each pixel electrode contacting one of the drain electrodes;
- a common electrode on a second substrate 16, the common electrode facing the first substrate; and
- a liquid crystal layer 20 interposed between the common electrode and the pixel electrodes.
- plurality of transparent layers (color filters) including light shielding color filter patterns filling a space between the thin film transistor and the liquid crystal layer

Art Unit: 2871

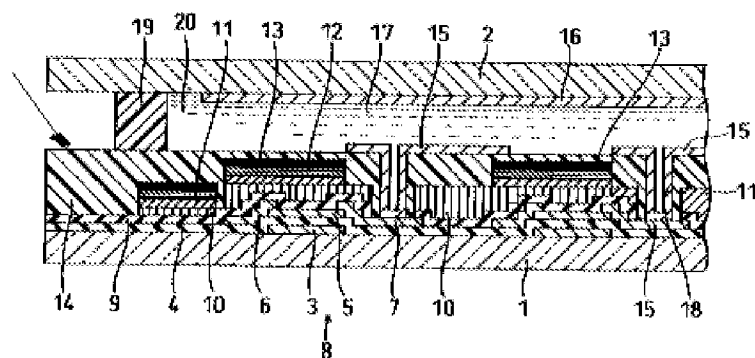
20, the light shield color filter color patterns including at least two of red, green or blue resins.

wherein

- thickness of the light-shielding color filter patterns is equal to or less than a thickness of the color filter.
- a top surface of the color filter substantially has the same level as a top surface of the light-shielding color filter patterns since the top surfaces of the color filter and light-shielding color filter patterns is the surface of the flattening film 14.

FIG. 2

top surface of color filters and top surface of light-shielding color filters pattern are the same



Claims 4 and 21:

- each thin film transistor includes a channel on the active layer between the source and drain electrodes.

Claims 5 and 22:

- the light-shielding color filter patterns are formed of the same material as the color filters.

Claims 6 and 23:

Art Unit: 2871

- a cell gap between the light-shielding color filter patterns and the common electrode is greater than zero.

Claims 7, 24, 39 and 48:

- the color filters are formed of a photosensitive resin through a photolithography process.

Claims 8, 25 and 37:

- red, green and blue color filters are formed sequentially from the semiconductor layers towards the liquid crystal layer.

Claims 9, 26, 38 and 50:

- each of red, green and blue color filter patterns (at shielding regions) has a thickness smaller than each of red, green and blue color filters (at display regions).

Claims 10 and 27:

- each light-shielding color filter pattern has a red color filter pattern, a green color filter pattern and a blue color filter pattern.

Claims 11, 28-29, 40 and 51-52:

- a second insulating layer between the thin film transistors and the light-shielding patterns and between the first insulating layer and the color filters, wherein the second insulating layer covers the source electrodes, the drain electrodes and the data lines and wherein the drain contact holes extend through the second insulating layer wherein performing etching an exposed portion of the second

insulating layer such that the drain contact holes extend through the second insulating layer to expose a portion of each drain electrode.

Claims 12, 30-31, 40, 52-54:

- a third insulating layer between the color filters and the pixel electrodes, wherein the third insulating layer covers the color filters and the light-shielding color filter patterns, wherein performing etching a portion of the third insulating layer corresponding to the drain contact holes such that the drain contact holes extend through the third insulating layer to expose a portion of each drain electrode.

Claim 45:

- each of the red, green and blue color filters includes a drain contact hole exposing the drain electrode and wherein the pixel electrode contacts the drain electrode through the drain contact hole 50.

Claim 49:

- the light-shielding color filter pattern is formed in the same process step as the color filter.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2-3, 19-20 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamamoto et al. (US6445432B2)** as applied to claims 1, 4-12, 18, 21-31, 35, 37-41 and 48-54 and in view of Shin (US5825449A).

**Yamamoto et al.** fail to disclose a liquid crystal display device comprising each semiconductor layer includes an active layer of amorphous silicon and an ohmic contact layer of doped amorphous silicon, wherein the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other.

Shin teaches (Figs. 2-3) a liquid crystal display device comprising each semiconductor layer includes an active layer of amorphous silicon 4 and an ohmic contact layer 5 of doped amorphous silicon, wherein the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other for reducing the contact resistance between the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as **Yamamoto et al.** disclosed with each semiconductor layer including an active layer of amorphous silicon 4 and an ohmic contact layer 5 of doped amorphous silicon, wherein the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other for reducing the contact resistance between the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).



3. Claims 13-17, 32-34 and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamamoto et al. (US6445432B2)** as applied to claims 1, 4-10, 18, 21-27, 35, 37-39, 45-46 and 48-50 and in view of Song (US6307602B1).

**Yamamoto et al.** further disclose a liquid crystal display device comprising colors filters covering gate lines.

**Yamamoto et al.** fail to disclose a liquid crystal display device comprising a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode on the first insulating layer over each portion of the gate line, wherein each second capacitor electrode and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode.

Song teaches (Fig. 4a-5f) a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode 150 on the first insulating layer (gate insulating layer 111) over each portion of the gate line, wherein each second capacitor electrode 150 and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode. Combination of **Yamamoto et al.** and Song (Figs. 4-5 show storage electrodes covering gate lines) inherences each color filter including capacitor contact hole exposing the second capacitor electrode, wherein the pixel electrode contact the second capacitor electrodes through the capacitor contact holes.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as **Yamamoto et al.** disclosed with a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode 150 on the first insulating layer (gate insulating layer 111) over each portion of the gate line, wherein each second capacitor electrode 150 and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode for high display quality with preventing shorting between pixel electrodes as Song taught (col. 2 lines 25-34).

### ***Conclusion***

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2871

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571)272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HOAN C. NGUYEN  
Examiner  
Art Unit 2871

Chn

/David Nelms/  
Supervisory Patent Examiner, Art Unit 2871